AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-7 (cancelled)

Claim 8 (currently amended): [[The]] A nonvolatile semiconductor memory device, ~~according to claim 5~~ comprising:

a memory cell array; wherein the memory cell array is constituted by arranging a plurality of memory cells comprising:

a plurality of variable resistive elements capable of storing information in accordance with a change of electrical resistances; and

a selection element for selecting the variable resistive elements in common; wherein one ends of the variable resistive elements are connected each other, and

an electrode of the selection element is connected with one end of each of the variable resistive elements;

the memory cells arranged like a matrix in a row direction and column direction and moreover, a word line is included in each row of the memory cells along the row direction, and bit lines extending along a column direction in each column and equal to the number of the variable resistive elements in the memory cells are included; and

wherein a hierarchical bit line structure is used in which at least a plurality of blocks is arranged in the column direction by using the memory cell array as one block, the bit line of each block is used as a local bit line, a local bit line selection transistor for selecting the local bit line is set, and the local bit line is connected to a global bit line through the local bit line selection transistor.

Claims 9-11 (cancelled)

Claim 12 (new): A nonvolatile memory cell, comprising:

a first and a second variable resistive element, each capable of storing information in accordance with a variance in electrical resistance, each variable resistive element having a first end and a second end, the first ends coupled;

the second end of the first variable resistive element coupled with a first bit line, and the second end of the second variable resistive element coupled with a second bit line;

one of a source and a drain of a transistor coupling with the first bit line and the other of the source and the drain coupling with the second bit line; and

a selection element for selecting the first and the second variable resistive element in common, the selection element having a first electrode coupled with the first ends.

Claim 13 (new): The nonvolatile memory cell according to claim 12, wherein each of the variable resistive elements is one of an RRAM element, an MRAM element, and an OUM element.

Claim 14 (new): The nonvolatile memory cell according to claim 12, wherein the selection element is a MOSFET and the first electrode of the selection element is one of a source and a drain, the selection element further comprising a gate.

Claim 15 (new): The nonvolatile memory cell according to claim 14, wherein the first bit line and the second bit-line are disposed substantially parallel to each other a predetermined distance apart, and wherein the gate of the selection element is disposed substantially perpendicular to the first and the second bit lines, the gate having a width at least as great as a sum of a width of the first bit line, a width of the second bit line, and the predetermined distance.

Claim 16 (new): The nonvolatile memory cell according to claim 12, wherein the selection element is a diode, and wherein the first electrode of the selection element is one of an anode and a cathode.

Claim 17 (new): A nonvolatile memory cell array, comprising:

a first and a second memory cell, each memory cell comprising:

a first and a second variable resistive element, each variable resistive element capable of storing information in accordance with a variance in electrical resistance, each having a first end and a second end, the first ends coupled, the second end of the first variable resistive element coupled with a first bit line, and the second end of the second variable resistive element coupled with a second bit line; and a selection element for selecting the first and the second variable resistive elements in common; and

a first global bit line coupling with the second bit line of the first memory cell and the first bit line of the second memory cell.

Claim 18 (new): The nonvolatile memory cell array according to claim 17, wherein the selection element of the first and the second memory cells is one of a MOSFET and a diode.

Claim 19 (new): The nonvolatile memory cell array according to claim 17, wherein the first global bit line couples with the second bit line through a first transistor and with the first bit line through a second transistor.

Claim 20 (new): The nonvolatile memory cell array according to claim 17, further comprising:

a second global bit line, the second global bit line coupling with the second bit line of the second memory cell;

a differential comparator circuit for outputting a result, the first and the second global bit lines inputting to the comparator circuit.

Claim 21 (new): The nonvolatile memory cell array according to claim 18, wherein the differential comparator generates a result for output without reference to a reference voltage.

Claim 22 (new): The nonvolatile memory cell array according to claim 20, further comprising:

a third memory cell, the third memory cell comprising:

a first and a second variable resistive element, each variable resistive element capable of storing information in accordance with a variance in electrical resistance, each having a first end and a second end, the first ends coupled, the second end of the first variable resistive element coupled with a first bit line, and the second end of the second variable resistive element coupled with a second bit line; and a selection element for selecting the first and the second variable resistive elements in common;

a third global bit line coupling with the second bit line of the third memory cell; and

wherein the second global bit line couples with the first bit line of the third memory cell.

Claim 23 (new): The nonvolatile semiconductor memory device according to claim 17, wherein each of the variable resistive elements is one of an RRAM element, an MRAM element, and an OUM element.